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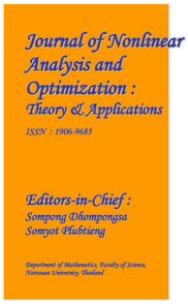

HIGH-SPEED, LOW AREA ARCHITECTURE OF 2-D BLOCK FIR FILTER USING DA

A SWETHA RANI[1], S M GANESH[2,] K PRAVEEN[3], KALIGAR MOHAMMED SABIYA BANU[4] [13]Assistant professor, [2]Associate Professor, [4]Student Department Of ECE Bheema Institute of Technology and Science, Adoni

Abstract:
Based on the multiply and accumulate block, this study suggests a novel block-efficient distributed arithmetic (DA) method for 2-D block FIR filters. For the DA lookup table (DALUT), a hardware-based design that enables reconfigurable 2-D FIR filter architecture is proposed. Block processing also leads to sharing at different stages amongst DA-LUTs. This would simplify the DA-LUT hardware by resulting in the construction of a single DA-LUT for block inputs. In addition, the proposed design reduces the systolic architectures compared to the previous designs by using memory overlapping. For higher-order 2-D FIR filters, the internal block is divided into small and parallel blocks, which reduces the DA-LUT complexity. The suggested design is compared with the previously published designs using the ASIC synthesis findings, and it is shown that the present design offers considerable improvements in various performance characteristics.

Keywords: distributed arithmetic, FIR filter,

1. Introduction

In a wide range of image and video processing applications, including image restoration, image enhancement, template matching, and video communication [1,2], two-dimensional (2-D) digital filters are frequently utilised. The numerical stability and ease of design of 2-D FIR filters make them preferred to IIR filters. Additionally, a FIR filter is a desirable option for applications that call for linear phase preservation. Due to the numerous computations involved, designing an effective 2-D FIR structure is a constant challenge for researchers. Parhi proposed a systolic structure for 2-D FIR filters in [3]. However, by utilising symmetry features, a significant portion of the computations necessary in [3] are decreased in [2, 4]. Recently, Mohanty proposed the 2-D block FIR filters' separable and non-separable structures. In these situations, the employment of DA-based approaches offers dynamic reconfigurability of filter coefficients, but the MCM-based techniques might not be suited for the same. Additionally, numerous scholars have put forth architectures for 1-D digital filters based on the DA notions and the references therein. To the best of the authors' knowledge, no literature has been documented on the architecture for 2-D block FIR filters utilising DA algorithm. This inspires us to complete the current work. Therefore, an unique DA-based systolic design for 2-D block FIR filters is suggested in this study. The suggested design uses DA-LUTs that are hardware-based (DA lookup table) and hardware complexity are decreased by the use of pipelining and parallelism. At each systolic step, a significant number of DA-LUTs are also shared, which lowers the amount of processing units in the architecture. Additionally, just a small portion of the architecture operates at the faster clock, which increases power efficiency.

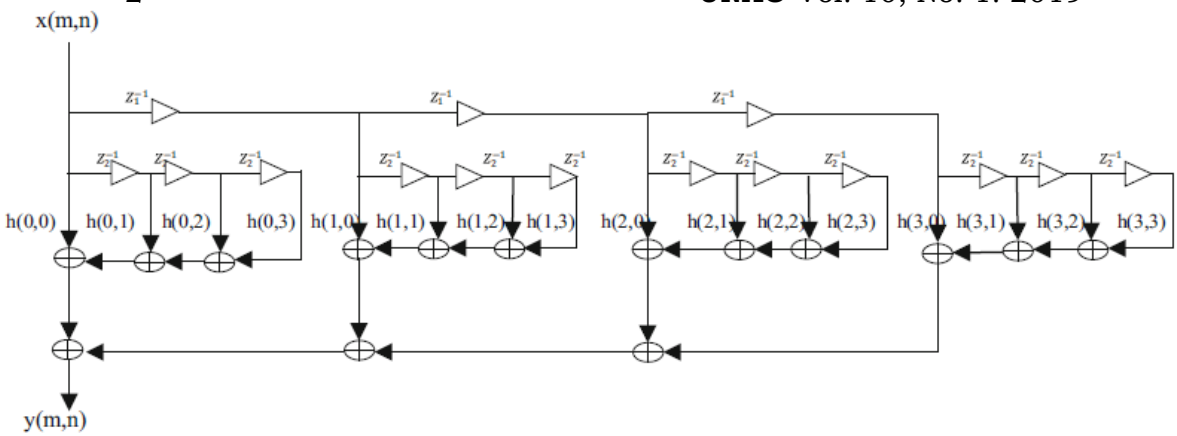

Fig.1 Direct form of FIR filter

2. Proposed Design

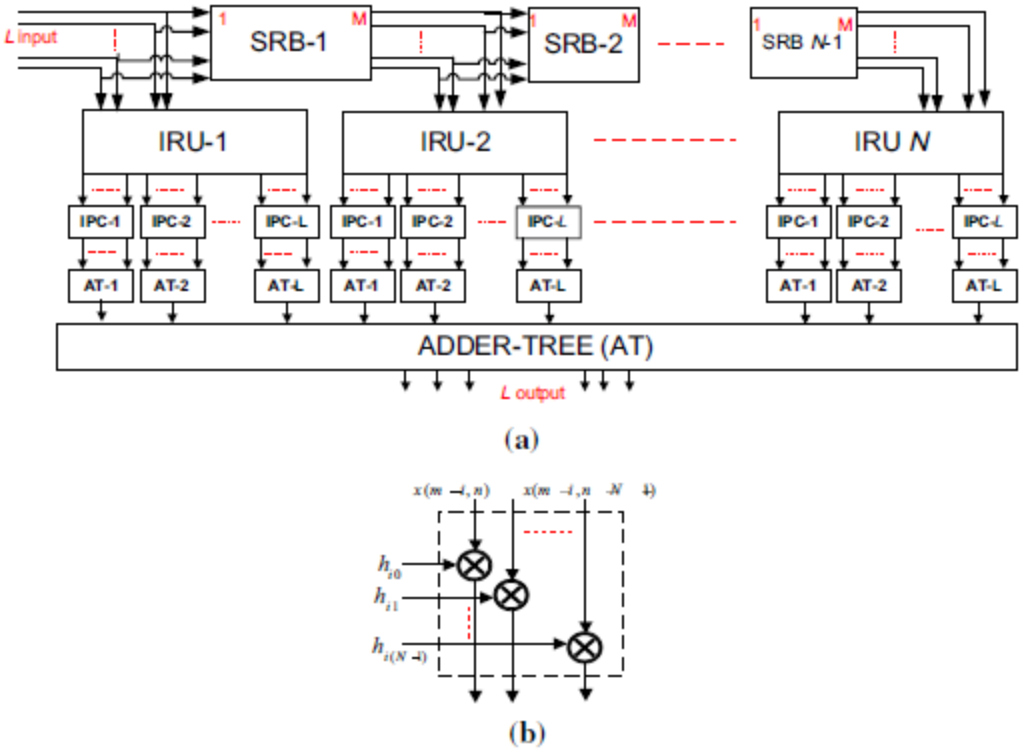

Fig.2.(a) Proposed design2(b) Inner product block

Since all the desired delayed-input samples are already present in the SRB block (see Fig. 2) at each systolic stage, internal systolic structures with respect to z1 (i.e., the IRU blocks) are not required. Therefore, the SRB block may immediately access these necessary delayed-input samples. Because the delayed-input samples needed for the last systolic stage (Nth systolic stage) cannot be retrieved directly from the SRB, an IRU block is only needed for this stage to provide the requisite input samples. Additionally, because all internal block outputs are added directly using the 2log2N-stage adders tree, the architecture in [4] (see Fig. 2) offers a longer critical path (AT).

3. Simulation Result

Table 1 lists the hardware and temporal complexities of the proposed design as well as previously published architectures [4] and [6] for the 2-D FIR filter. It is clear that [4] and [9] require numerous multipliers, which take up the majority of the chip surface, whereas the suggested architecture is a multiplier-less design.Additionally, the proposed architecture requires fewer normalised registers per

input than [4] but a bit more than [9]'s architecture. The entire design is divided into two halves, input stage and output stage, as a result of mid-stage pipelining**.**

Table.1 Synthesis results for 16-tap filter

Design	**Area(μm2)**	**Power(mw)**	**Time(ns)**
Ref[4]	**1400**	**19**	**13**
Ref[6]	**2455**	**50**	**11**
Proposed design	**1231**	**20**	**6**

4.Conclusion:

In this study, we have analysed the limitations of the existing design of the 2-D block FIR filter [9] and examined possible enhancements. After that, we provided a helpful DA formulation for the construction of a 2-D FIR filter intended for block processing. The amount of memory required to realise the concept has lowered due to memory overlapping. Furthermore, a successful DA-LUT sharing method is used to minimise the number of DA-LUTs; this method decreased the number of DA-LUTs by 76.50% for N = 16, L-16, and p 4.

References:

1. D.J. Allred, H. Yoo, V. Krishnan, W. Huang, D.V. Anderson, LMS adaptive filters using distributed arithmetic for high throughput. IEEE Trans. Circuits Syst. I Reg. Pap. **52**(7), 1327–1337 (2005)
2. P.Y. Chen, L.D. Van, H.C. Reddy, I.H. Khoo, Area-efficient 2-D digital filter architectures possessing diagonal and four-fold rotational symmetries, in Proceedings of the International Conference on Information, Communications and Signal Processing (ICICS) (Tainan, Taiwan, 2013), pp. 1–4
3. R. Guo, L.S. DeBrunner, Two high-performance adaptive filter implementation schemes using distributed arithmetic. IEEE Trans. Circuits Syst. II Exp. Briefs **58**(9), 600–604 (2011)
4. I.H. Khoo, H.C. Reddy, L.D. Van, C.T. Lin, Generalized formulation of 2-D filter structures without global broadcast for VLSI implementation, in Proceedings of the IEEE MWSCAS (Seattle,WA, USA, 2010), pp. 426–529
5. P. Kumar, P.C. Srivastava, M. Tiwari, A. Dhawan, ASIC implementation of area efficient highthroughput2-D IIR filter using distributed arithmetic. Circuits Syst. Signal Process. **37**(7), 2934–2957 (2018). https://doi.org/10.1007/s00034-017-0698-z
6. X. Lou, Y.J. Yu, P.K. Meher, Lower bound analysis and perturbation of critical path for area-time efficient multiple constant multiplications. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. **36**(2), 313–324 (2017)